REMARKS/ARGUMENTS

Claims 1-20 are pending in the application; reexamination and reconsideration are hereby requested.

Figs. 4-5 were objected to because element 24 in Fig.5 did not show the output as in Fig.4.

Applicant replies that Fig.5 is a flowchart which includes the functioning in element 24 of functional block diagram Fig.4, and in Fig.5 the output ($O_F[n]$) is written to registers in step 44. That is, the reference number "24" in Fig.5 refers to the functioning in block "24" in Fig.4.

Paragraphs [003]-[004] have been amended to correct the reference numbers to match those of Fig.1

Claims 9-16 were objected to for informalities. The claims have been amended as suggested by the Examiner.

The specification was objected to because claims 6 and 18 referred to the line rate with respect to the offset and gain updating rate, but the description only refers to the frame rate. The claims have been amended to only refer to the frame rate.

Claims 17-20 were rejected as indefinite due to "the amplitude of the video signal" and two different signals called video signals. Claim 17 has been amended to clarify the signals.

Claims 1-4 and 17 were rejected as anticipated by Jennes.

Applicant replies that Jennes has a sync gain and sync threshold set by a searching method as illustrated in Fig.4 and col.8, ln.49 to col.9, ln.43, not a feedback updating method, and this finds the back porch/blanking level. Further, the video gain and video offset are computed just to make full use of the ADC input range, see col.11, ln.6-22, not to adjust the video signal. This does not suggest the offset adapted to the gain as required by claim 1. Amended independent claim 17 further requires both the analog gain and offset plus the digital gain and offset.

Claims 5-8 and 18-20 were rejected as unpatentable over Jennes.

Applicant relies upon the patentability of parent claims 1 and 17.

Respectfully submitted,

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